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(54) Parallel Operation Method of Inverters, Inverter Power Source Unit used for the Method and Inverter Power Source Unit for Charging Lamp Lighting

(57) [Abstract]

[Object] It is to inhibit currents with a high frequency generated in an inverter to flow to an electric power source that supplies electric power to the inverter in an inverter power source unit that generates AC power with a frequency higher than

a commercially-available frequency by means of an inverter to operate a load.

[Means for Achieving the Object] When inverters in total of M · N (M is an integer of 2 or more, N is an integer of 1 or more) are operated in parallel, the inverters are divided into 3 groups, and the inverters of the respective groups are operated with holding a phase difference of 360° /M or 180° /M to average the instant current values of currents flowing to the electric power source side.

[Claims]

[Claim 1] A parallel operation method of inverters characterized in that, in an electric power source unit in which electric power is supplied from a common electric power source to a plurality of inverters, AC power with a frequency higher than a commercially-available frequency is generated by the respective inverters, and the AC power is supplied to respective loads to operate the loads, a drive phase of the respective inverters is shifted to average instant current values of currents flowing to the electric power source side.

[Claim 2] A parallel operation method of inverters according to claim 1, characterized in that the number of the inverters is fixed to M・N (M is a positive integer of 2 or more, and N is a positive integer of 1 or more), the inverters in total of M・N are divided in M groups, and the inverters in the respective groups are operated with holding a phase difference of 360° /M or 180° /M.

[Claim 3] An inverter power source unit characterized by comprising;

A. an AC power reception terminal for receiving AC power with a commercially-available frequency;

B. a full wave rectification circuit for rectifying the AC power having been received to the AC power reception terminal;

C. a smoothing circuit for smoothing the rectified power having been rectified in the full wave rectification circuit;

D. an inverter for converting the DC power having been smoothed in the smoothing circuit to AC power with a frequency higher than a frequency of the AC power having been received to the AC power reception terminal;

E. a sending terminal for supplying the converted power by the inverter to a load;

F. a drive signal generating means for providing a drive signal to the inverter; and

G. a phase fixing means for fixing a drive phase of the drive signal generating means to a reference phase or the other phase.

[Claim 4] An inverter power source unit characterized by comprising;

A. an AC power reception terminal for receiving AC power with a commercially-available frequency;

B. a full wave rectification circuit for rectifying the AC power having been received to the AC power reception terminal;

C. a smoothing circuit for smoothing the rectified power having been rectified in the full wave rectification circuit;

D. inverter in total of M for converting the DC power having been smoothed in the smoothing circuit to AC power with a frequency higher than a frequency of the AC power having been received to the AC power reception terminal;

E. a sending terminal for supplying the respective converted power by the inverters in total of M to a load; and

F. M sets of drive signal generating means for providing a drive signal having a phase difference of 360° /M or 180° /M to the respective inverters in total of M.

[Claim 5] An inverter power source unit characterized by comprising;

A. a DC power reception terminal for receiving DC power;

B. an inverter for converting the DC power to be received to the DC power reception terminal to AC power with a frequency

higher than a commercially-available frequency;

C. a sending terminal for supplying the AC power having been converted in the inverter to a load;

D. a smoothing circuit being inserted between the DC power reception terminal and the inverter and for smoothing a load current to be supplied to the load;

E. a drive signal generating means for supplying a drive signal to the inverter; and

F. a phase fixing means for fixing the drive phase of the drive signal generating means to a reference phase or the other phase.

[Claim 6] An inverter power source unit characterized by comprising;

A. a DC power reception terminal for receiving DC power;

B. an inverter for converting the DC power to be received to the DC power reception terminal to AC power with a frequency higher than a commercially-available frequency;

C. M sets of sending terminals for supplying the AC power having been converted in the inverters in total of M to loads;

D. a smoothing circuit being inserted between the DC power reception terminal and the inverters in total of M and for smoothing load currents to be supplied to the respective loads; and

E. M sets of drive signal generating means for supplying a drive signal having a phase difference of 360° /M or 180° /M to the respective inverters in total of M.

[Claim 7] An inverter power source unit according to any one of claims 3 to 6, characterized in that the unit is used for charging lamps and is configured by additionally including a

boost transformer, a filter and a charging lamp start-up circuit respectively for lightening charging lamps between the inverter and the sending terminal.

[Detailed Explanation for the Invention]

[0001]

[Field of the Invention]

The present invention relates to a parallel operation method of inverters suitably used for lighting a plurality of charging lamps, for example, lights for luring fish, an inverter power source unit used for the method, and an inverter power source unit for charging lamp lighting use.

[0002]

[Prior Art]

In fishing grounds, metal halide lamps (charging lamps) having high brightness and high luminous efficiencies have been used dominantly in recent years, instead of incandescent lamps comprising lights for luring fish. As shown in FIG. 15, a power source unit UN that lightens the lights for luring fish is configured with AC power reception terminal T_{INAC}, a boost transformer T, a filter F, a start-up circuit ST and a sending terminal T_{OUT} for connecting a charging lamp that is a load. In order to lighten a charging lamp L made from a metal halide lamp, AC power with 60 Hz, that is one of commercially-available electric power frequencies, is supplied from, for example, a generator G to the boost transformer T via the AC power reception terminal T_{INAC}, and the boosted AC power is impressed to a charging lamp L.

[0003]

This power source unit UN has demerits of requiring a large magnetic core and having quite a heavy weight, since the boost transformer T and the filter F to be used for the power source unit have been made for the use with 60 Hz. For example, nearly a hundred lamps are installed on a squid fishing boat, and in such a small fisherboat, miniaturization and reduction in weight of an electric power source unit to be used for lamps for luring fish are intensively desired. As one method for solving the above-mentioned problem, an electric power source unit UNV using an inverter INV as shown in FIG. 16 has been proposed. This electric power source unit comprises an AC power reception terminal T_{INAC}, a rectification circuit REC for rectifying the AC power with a commercially-fixed frequency having been received from the AC power reception terminal T_{INAC}, a smoothing circuit W for smoothing the rectified electric power by the rectification circuit REC, an inverter INV for converting the smoothed output power from the smoothing circuit W into the AC power having a frequency being higher than the commercially-available frequency, a boost transformer T for boosting a voltage of the AC power outputted from the inverter INV, a filter F for approximating the wave form of the boosted electric power to the sine wave form, a start-up circuit ST for starting up a charging lamp being a load, a sending terminal T_{OUT} for supplying the AC power generated in the inverter INV to the charging lamp L being a load, and a drive signal generating means OS for providing a drive signal to the inverter INV.

[0004]

As publicly known, the inverter INV is operated such that, for example, a series connection configured by connecting

insulated-gate bipolar transistors (hereinafter referred to as IGBT) Q1 and Q2 and a series connection configured by connecting IGBTs Q3 and Q4 are connected in parallel, a primary coil of the boost transformer T is connected to between the respective connection points of the series-connected IGBTs Q1 and Q2 and the series-connected IGBTs Q3 and Q4, and a state where the IGBTs Q1 and Q4 being conducted and a state where the IGBTs Q2 and Q3 being conducted are repeated alternately to thereby impress an AC voltage to the boost transformer T.

[0005]

The IGBT comes to be in the state of being turned on during a period where, for example, pulses with positive polarity are impressed to gate electrodes. Accordingly, drive signals S_{G1} to S_{G4} as shown in FIG. 17 are supplied to the respective gate electrodes G1 to G4 of the IGBTs Q1 to Q4 comprising the inverter INV. That is, the drive signals S_{G1} and S_{G4} is supplied to the gate electrodes G1 and G4 of the IGBTs Q1 and Q4 in the same phase, and the drive signals S_{G2} and S_{G3} are supplied to the gate electrodes G2 and G3 of the IBGTs Q2 and Q3. Depending on a time required for generating drive signals S_{G1} and S_{G4} and a time T2 required for generating drive signals S_{G2} and S_{G3}, a frequency f_0 of an AC power to be impressed to a charging lamp being a load. In this example, an explanation will be made for a case where it is assumed that a frequency of AC power generated by an AC power source (a generator G in this example) is 60 Hz and a frequency of AC power with which six times the AC power, that is 360 Hz, is supplied to the load is f_0. The respective drive signals S_{G1} to S_{G4} are formed by generating a plurality of pulse-width-modulated pulses during the time T1 and the time

T2, respectively. The pulse width modulation is performed in accordance with a sine wave form such that the outputted current comes to a maximum pulse width in the respective middle regions of the times T1 and T2 so that the outputted current approximates to a sine wave.

[0006]

An example of the drive signal generating means OS is shown in FIG. 19. The drive signal generating means OS is configured by, for example, an oscillator OSC for generating clock pulses having a frequency being six times the frequency of the AC power (in this example, 60×6=360 Hz) generated by the generator G being an AC power source and an address counter ADRC for counting the number of the clock pulses generated by the oscillator OSC to access to a wave form memory WFM.

[0007]

The wave form memory WFM may be formed with, for example, a read only memory (ROM), and just one cycle portion (T1+T2) of the drive signals S_{G1} to S_{G4} as shown in FIG. 17 is stored in the address order into the wave form memory WFM. The address counter ADRC may be formed with, for example, a ring counter and generates addresses from the leading address till the final address being stored in the wave form memory WFM repeatedly corresponding to the number of pulses supplied from the oscillator OSC.

[0008]

When the read-out of the drive signals S_{G1} to S_{G4} from the wave form memory WFM is performed at a read-out resolution, for example, equally divided by 10 during a time (T1+T2), an oscillation frequency of a voltage control oscillator VCO comes

to 360×10=3.6 KHz, and via an equation of 3.6 KHz/J=60 Hz, a frequency division number 1/J of a frequency divider is given as J=60. The drive signals S_{G1} to S_{G4} as shown in FIG. 17A are supplied to the inverter INV, and the IGBT Q1, Q2 and Q3 are turned on and off alternately so that the pulse voltage shown in FIG. 17B is impressed to the primary coil of the boost transformer. The pulse voltage VP is impressed to a series circuit consisting of the filter F and the charging lamp L, and as a result, an output current I_0 in a sine wave state as shown in FIG. 17C flows into the charging lamp L. The frequency f_0 of the current I_0 comes to a value that is determined by the synchronization (T1+T2) of the drive signals S_{G1} to S_{G4}, that is f_0=360 Hz.

[0009]

Upon the flowing of the current I_0 as the output current from the inverter INV, a pulsating current I_{DC} as shown in FIG. 17D, that is obtained by the both waves rectification of the output current I_0, flows into the input side of the inverter INV, and a current I_{AC} (FIG. 18B) having a frequency of $2f_0$, that is a summed frequency of both the positive half cycle and negative half cycle of an AC-power AC (FIG. 18A) generated by the generator G, flows into the input side of the rectification circuit, that is the generator G.

[0010]

[Object to be achieved by the Invention]

In response to the flowing of a current I_{AC} having a high frequency as shown in FIG. 18B into the generator G, such a drawback that the power-factor in the generator G is lowered to thereby decrease the effective output capacity is caused.

Furthermore, a local heat generation is caused in a rotor coil and the like, it is required to decrease the load factor to a great extent. Therefore, there is such a disadvantage that a generator with a power capacity being greater than the apparent load capacity must be used.

[0011]

Further, even when a battery is used for the electric power source, such a drawback that heat generation is occurred at the time of taking out a current with a high frequency from the battery and of shortening the longevity of the battery. In order to eliminate such a drawback, it is also possible to use an active filter AF provided with an active element as shown in FIG. 20. This active element has a feedback circuit that changes an input current into sine waves and exerts a function of suppressing higher harmonics.

[0012]

However, the installation of the active filter AF causes an increase in the cost, and it is unavoidable for the apparatus to be large in the size and heavy in the weight. Therefore, it is an object of the present invention to provide a parallel operation method of the inverters with which a current with a high frequency flowing into the electric power source side can be easily suppressed, an inverter power source unit to be used for said method, and an inverter power source unit for charging lamp lighting use.

[0013]

[Means for Achieving the Object]

The parallel operation method of inverters according to the present invention comprises providing a plurality of

inverter power source units, driving the plurality of inverter power source units in different phases from one to another, and operating a plurality of inverters so that the instant values of currents flowing into the electric power source side are averaged by the difference in the phases.

[0014]

The higher harmonic components may be decreased to a great extent by averaging the instant values of currents flowing into the electric power source side. As a result, for example, when the generator is used, an advantage being capable of rendering the power capacity of the generator smaller may be attained because the power-factor may be greatly improved. Even when a battery is used, heating generation in the battery may be suppressed and the shortening in the longevity of the battery may be prevented from occurring because the higher harmonic components contained in the currents flowing in the battery may be decreased.

[0015]

When inverters in total of an even number are operated in parallel, the inverters in total of an even number are divided into two, and one group thereof and the other group thereof may be operated in parallel such that the both groups form a phase difference of about 90° between their phases. In such a situation under the parallel operation, the instant values of currents with a frequency of $2f_0$ flowing in the generator may be averaged because there is an anti-phase relation between the two groups such that one group comes to the minimum value when the other group comes to the maximum value. That is, the currents become currents with less pulsation (ripple), whereby the

content of the higher harmonic components may be decreased.

[0016]

When the inverters in total of a number given by multiplying 3 with an integer are operated in parallel, the inverters in total of that number are divided into 3 groups, and the respective groups are operated in parallel such that the respective phases of those groups are shifted by 120° from one to another. In such a situation under the parallel operation, an advantage of further decreasing the ripples of currents flowing in the generator and further lowering the content of higher harmonic components may be attained because the respective currents with a frequency of $2f_0$ flowing in the generator have a phase difference of 120° from one to another.

[0017]

The number of the inverter may be generalized into M · N. M may be defined as the number of the inverters to be operated in parallel and is an integer of 2 or more, and N may be defined as the number of the inverters to be assigned to the respective groups of the inverters to be operated in parallel and is an integer of 1 or more. Accordingly, the inverters in total of M · N may be divided into M groups, and the inverters divided into M groups may be given with a phase difference of 360° /M or 180° /M from one to another and are then operated.

[0018]

Provided, when being M=2, the phase difference between the inverters divided into two groups comes to be 90° only, but when being M=3, the phase difference may 120° or 60° as described above. That is, when the rectification circuit REC is a full wave rectification circuit, the phase difference of

the pulsation that flows following to the full wave rectification comes to be 60° irrespective of shifting the phases of the inverters divided into 3 groups by 120° to then operate or shifting said phases by 60° to then operate.

[0019]

Accordingly, when being M=4, the phase difference to be provided to the inverters may be either 360° /4 or 180° /4. Besides, the number of the parallel operations of the inverters may be fixed to more than 4, and the ripples in the currents flowing at the electric power source side may be less with increasing the number of M. The inverter power source unit having a first configuration (corresponding to claims 3 and 5) according to the present invention is characterized by each including an inverter, a drive signal generating means for providing drive signals to the inverter, and a phase fixing means for fixing the phases of the drive signals generated by the drive signal generating means to a reference phase (0 phase) or the other phase.

[0020]

With the inverter power source unit having a first configuration, the drive phase of the inverter can be fixed with coordinating with the number of the inverter power source units having been connected to an electric power source, and therefore, an advantage of permitting the inverter power source unit to be used practically for both of the even parallel and odd parallel operations may be attained. The inverter power source unit having a second configuration (corresponding to claims 4 and 6) according to the present invention is characterized in that inverters in total of M are installed in the unit and the

inverters in total of M are driven in such a state that they respectively have a phase difference of 360° /M or 180° /M from one to another.

[0021]

With the inverter power source unit having the second configuration, it is possible to establish the optimum parallel operation by only an operation of connecting the respective inverter power source unit to an electric power source and connecting a load, since the inverters in total of M are incorporated so as to operate with holding a phase difference of 360° /M or 180° /M from one to another in the respective inverter power source unit. As a result, an advantage of permitting the inverter power source unit in the practical application to be handled easily may be attained.

[0022]

[Embodiments]

In FIG. 1, a block diagram for explaining the parallel operation method of the inverter proposed in claim 1 for the present patent application is illustrated. In FIG. 1, a generator F for AC use is used as an electric power source. In this example, the inverters in total of an even number are operated in parallel. That is, as a specific example, the parallel operation method of the inverters proposed in claim 2 wherein the total operation number M of the inverters is fixed to 2 will be explained in the following. In this example, it is assumed that M is 2, n is 1, and two inverter power source units are used. These two inverter power source units respectively lighten a charging lamp L as being a load. In this example, in order to lighten a charging lamp L, a boost

transformer T for generating a requisite voltage for lightening the charging lamp L and a start-up circuit ST for starting-up the charging lamp L are installed in the unit at the sending terminal T_{OUT} side.

[0023]

In the parallel operation method of the inverters, two inverter power source units are operated in parallel in such a manner that the two units form a phase difference of 90° (180° /M) from each other. In order to achieve such a parallel operation, it is characteristically configured such that, in one of the two inverter power source units 10, a synchronizing signal obtained by wave-form-fairing in the wave form fairing circuit WFO is directly inputted to a drive signal generating means OS and the inverter INV is driven at the reference phase having been synchronized to an AC voltage signal generated by a generator G, while in the other of the two inverter power source units 10, a synchronizing signal obtained by wave-form-fairing is inputted to the drive signal generating means OS through a delay circuit DY1 that causes the phase of the synchronizing signal to delay by only about 90° (or 270°). With the configuration including the delay circuit DY1, it is possible to operate the two inverter power source units with maintaining the phase difference of about 90° .

[0024]

As a result of driving the two inverters INV with maintaining the phase difference of about 90° , a current I_{01} and a current I_{02}, whose phases are different from each other, flow into the charging lamp L as being a load, as shown in FIG. 2A. As explained in FIG. 17, these currents I_{01} and I_{02} may be

fixed to, for example, 360 Hz, that is determined by a cycle (T1+T2) of the drive signals S_{G1} to S_{G4} generated in the drive signal generating means OS.

[0025]

As a result of flowing of the currents I_{01} and I_{02} having phases differing by 90° from each other to a load, rectified currents I_{B1} and I_{B2} as shown in FIG. 2B flow into the output side of the rectification circuit REC, namely a smoothing circuit W. These rectified currents I_{B1} and I_{B2} are in an anti-phase relation where one of the rectified currents comes at the minimum value when the other is at the maximum value. Accordingly, a synthesized current flowing to a common generator G, wherein the portions of the wave valleys of the two currents are superimposed to cause smoothing, becomes a current having less ripples. In FIG. 3, a wave form of an AC current I_{AC} to be taken out of the generator G is shown. The ripple RP is a resultant ripple of the portions of the rectified currents I_{B1} and I_{B2} as shown in FIG. 2B.

[0026]

As can be seen from the wave form of the rectified current I_{AC} shown in FIG. 3, the higher harmonic components of the rectified current I_{AC} is greatly decreased in comparison with the AC current I_{AC} shown in FIG. 18. That is, a component with a frequency of 60 Hz of the basic wave is the maximum, and the higher harmonic components come to at a level lower than the level of the basic wave. Hence, an adverse influence caused by the higher harmonics to the generator G may be lowered. Although it was explained in the above for the case wherein M is fixed to 2 and N is fixed to 1, it will be readily appreciated that

there is no limitation in the number of the inverters as far as it is within the capacity of the generator G, by dividing the inverters in total of an even number into two groups when N is fixed to 2 or more.

[0027]

FIG. 4 is a block diagram for explaining the parallel operation method of inverters being proposed in claim 2 of this patent application, wherein the parallel operation number M of the inverters is fixed to 3 and N is fixed to 1. Therefore, in the example shown in FIG. 4, three inverter power source units 10 are installed, and the three inverter power source units are operated under such a state that their phases are shifted by about 120° from one to another.

[0028]

In order to realize the operation in this example, the inverter parallel operation method is formed such that the first inverter power source unit 10 directly inputs a synchronizing signal from a wave form fairing circuit WFO to a drive signal source OS and causes the signal to operate at a reference phase having been synchronized to an AC voltage generated by an AC generator G, the second inverter power source unit 10 supplies the synchronizing signal outputted from the wave form fairing circuit WFO to the drive signal generating means OS through a delay circuit DY2 for delaying said synchronizing signal by 120° , and the third inverter power source unit 10 supplies rectangular waves outputted from the wave form fairing circuit WFO to the drive signal generating means OS through a delay circuit DY3 for delaying said rectangular waves by 240° . When the frequency of the output current from the inverter INV is 360° , the delay

time τ_2 by the delay circuit DY2 for delaying the signal by 120° is given by an expression, $\tau_2=(1/360\ \text{Hz})(120°/360°)\fallingdotseq 0.926\ \text{ms}$, and the delay time τ_3 by the delay circuit DY3 for delaying the signal by 240° is given by an expression, $\tau_3=(1/360\ \text{Hz})(240°/360°)\fallingdotseq 1.00\ \text{ms}$.

[0029]

As a result of operating the three inverters while shifting their phases by 120° from one to another, currents I_{01}, I_{02} and I_{03} shown in FIG. 5A flow into the respective charging lamps L. These currents I_{01} to I_{03} become a three-phase AC current having a phase difference of 120°, respectively. The respective currents I_{01}, I_{02} and I_{03} flow at the input side of the respective smoothing circuit W as rectified currents I_{DC1}, I_{DC2} and I_{DC3} as shown in FIG. 5B. Since the rectified currents I_{DC1} is associated with the rectified current I_{DC2} and ID_{C3}, respectively and then flows into the AC generator G, a current I_{AC} as shown in FIG. 6 is taken out of the AC generator G. Since the current I_{AC} is a resultant current of the rectified currents I_{DC1} to I_{DC3} being in three phases, the ripple RP thereof is smaller than the ripple of the AV current shown in FIG. 3. Hence, the higher harmonic components contained in the current other than the basic waves may be reduced more than the current shown in FIG. 3, whereby an advantage of reducing adverse influence onto the generator G may be attained. Note that, an example where an AC generator G is used as an electric power source is explained above, a DC power source may be used as well in the inverter parallel operation method according to this invention. Since the amount of the higher harmonic components contained in the current to be taken out of a battery is reduced when the current is DC (i.e.,

a battery) as well, an advantage of reducing adverse influence onto the battery may be attained. Note that, as it is apparent from FIG. 5B, the phase difference of the full-wave-rectified currents I_{DC1}, I_{DC2} and I_{DC3} is 60° . As a result, it is appreciated that the same result may be obtained in both cases of operating the three inverters INV under the phase difference of 60° and 120° .

[0030]

FIG. 7 shows an example of the inverter power source unit being proposed in claim 3 of this patent application. In this example, an AC generator G is used as the electric power source. Hence, the inverter power source unit 10 includes an AC reception terminal T_{INAC} and a full wave rectification circuit REC, and the unit is configured such that an AC power is rectified to once convert into a DC power, and the DC power is impressed to the inverter INV after passing through a smoothing circuit W.

[0031]

The inverter power source unit 10 proposed in claim 3 is configured such that it can be applied to both of the parallel operation for the inverters in total of an even number and for the inverters in the total number of an odd number. That is, the inverter power source unit 10 in this example is characterized by including a first delay circuit DY1 having a delay amount equivalent to 90° , a second delay circuit DY2 having a delay amount equivalent to 120° , a third delay circuit DY3 having a delay amount equivalent to 240° , and a phase fixing means 11 for selecting an output from the respective delay circuits or an output from a wave form fairing circuit WFO to fix a drive phase of the inverter INV, in addition to the wave

form fairing circuit WFO.

[0032]

With the inverter power source unit in which it is configured such that synchronizing signals having the respective delay amounts may be selectively supplied to the drive signal generating means, it is possible to freely set the respective inverter power source units so as to be used in a desired phase corresponding to the number of the inverter power source units to be connected to the generator G. That is, when the inverter power source units 10 in total of an even number are operated, the inverter power source units of the even number may be divided into two groups, a phase fixing means 11 of the unit 10 in one of the two groups may be set to a change-over position 1, and a phase fixing means of the unit 10 in the other of the two groups may be set to a change-over position 2.

[0033]

When the inverter power source units in total of a number given by multiplying 3 by an integer are operated, the inverter power source units 10 of the number are divided into 3 groups, then a phase fixing means 11 of one of the three groups is set to a change-over position 1, a phase fixing means 11 of one of the other two groups is set to a change-over position 3, and a phase fixing means 11 of the rest of the other two groups is set to a change-over position 4, whereby the inverters of the respective groups may be operated with holding a phase difference of 120° from one to another and may structure an optimum condition for the parallel operation.

[0034]

Note that, although 90° , 120° and 240° are exemplified

in FIG. 7 as fixable phase difference, it is also possible to configure such that the inverter power source units are provided with the delay circuit having a delay amount corresponding to the value of the number M of the inverters INV used for the respective parallel operation, namely, 360° /3 and 180° /3 when being M=3, 360° /4 and 180° /4 when being M=4, 360° /5 and 180° /5 when being M=5, 360° /6 and 180° /6 when being M=6, and so on.

[0035]

FIG. 8 shows an example of the inverter power source unit proposed in claim 4 of this patent application, wherein the number M of the inverters used for the parallel operation is fixed to 2. Likely to the example shown in FIG. 7, the inverter power source unit 10 proposed in claim 4 is provided with an AC power reception terminal T_{INAC} and a full wave rectification circuit REC, and is further installed with two inverters in a common housing (in the unit) since M is fixed to 2, and the unit 10 is configured such that the two inverters are operated with holding a phase difference of 90° from each other.

[0036]

In this example, the two inverters INV are driven by a synchronizing signal outputted from a common oscillator OSC. That is, one of the two inverters INV directly receives the synchronizing signal having been outputted from the oscillator OSC by means of an address counter ADRC, generates an address signal having a reference phase, provides the address signal to the wave form memory WFM to generate a drive signal having the reference phase, and is driven.

[0037]

The other inverter causes the synchronizing signal generated in the oscillator OSC to delay by means of the delay circuit DY1 that gives a phase difference of 90° , provides the delayed synchronizing signal to the address counter ADRC, then further provides the address signal generated in the address counter ADRC to the wave form memory WFM to thereby generate a drive signal, and is driven by the drive signal. In order to realize the operation described above, the inverter power source unit is configured such that a synchronizing signal functioning as the reference phase is provided from the wave form fairing circuit WFO to one of the drive signal generating means OS that drives the two inverters, and a synchronizing signal outputted from the wave form fairing circuit WFO is provided to the other drive signal generating means OS through the delay circuit DY1 having a delay time equivalent to 90° .

[0038]

As described above, as a result of operating the two inverters INV inside the respective inverter power source units 10 with holding a phase difference of 90° , the currents flowing to the generator G are averaged and formed into currents containing less higher harmonics. Therefore, with the inverter power source unit 10 proposed in claim 4, an optimum parallel operation condition may be structured by simply connecting the inverter power source unit 10 to the generator G irrespective of the number of the inverter power source units to be connected to the generator G.

[0039]

FIG. 9 shows an example for the inverter power source unit proposed in claim 4, wherein M is fixed to 3. In this example,

likely to the examples shown in FIGS. 7 and 8, the inverter power source unit 10 is provided with, in addition to an AC power reception terminal T_{INAC} and a full wave rectification circuit REC, three inverters in a common housing since M is fixed to 3 and is configured such that the unit causes the three inverters to operate with shifting the phases of the respective inverters INV by 120° from one to another.

[0040]

In order to realize the configuration described above, the inverter power source unit is configured such that a synchronizing signal having the reference phase is provided from the oscillator OSC to the address counter ADRC of the wave form memory WFM that provides a drive signal to the first inverter INV, a synchronizing signal outputted from the oscillator OSC is supplied to the second inverter INV through a delay circuit DY2 having a delay time equivalent to 120° , and a synchronizing signal is provided to the third inverter INV through a delay circuit DY3 having a delay time equivalent to 240° .

[0041]

With the configuration as described above, as explained in FIGS. 5 and 6, since the wave form of a current flowing from the generator G to the inverter power source unit 10 becomes a current with less higher harmonics because of the averaging of the instant current values, an optimum parallel operation condition may be structured by simply connecting the inverter power source units of which number is as many as connectable within a range of the capacity of the generator G to the generator G.

[0042]

FIG. 10 and the afterwards show examples for inverter power source units of the DC reception type. The example shown in FIG. 10 is the inverter power source unit proposed in claim 5 of this patent application. This inverter power source unit of the DC reception type includes a DC reception terminal T_{INDC}, and a smoothing circuit W is directly connected to the DC reception terminal T_{INDC}, whereas a rectification circuit REC is omitted in this example.

[0043]

The inverter power source unit 10 of the DC reception type shown in FIG. 10 is equivalent to the inverter power source unit of the AC reception type shown in FIG. 7, however, the unit of FIG. 10 is considerably different from the unit of FIG. 7 in such a point that a synchronizing signal generator PG functioning as a synchronizing signal source and a synchronizing signal output terminal T_{SY} for sending out a synchronizing signal outputted from the synchronizing signal generator PG are further provided therein. In FIG. 10, a configuration of two inverter power source units is shown for convenience' sake. Duplex change-over switches 11A and 11B are used as a phase fixing means, and the change-over switches 11A and 11B are set to a change-over position 1 when causing the switches to operate in the reference phase. In FIG. 10, such a state that the upper inverter power source unit 10 is set as a unit that operates in the reference phase and the lower inverter power source unit is set as a unit that operates in the phase with delay of 90° is shown. Although a synchronizing signal generator PG is provided to the respective inverter power source units, when the inverter power source units are operated in a pair, one of the inverter power source units

10 in a pair is set such that it receives a supply of a synchronizing signal from the other inverter power source unit 10 to operate. This setting is performed by means of the change-over switch 11B. If the change-over switch 11B is set to a change-over position 1, a mode to sensing out a synchronizing signal to the other inverter power source unit is set. When the change-over switch 11B is set to a change-over position 2, a mode to supply a synchronizing signal having been sent from the other unit to the drive signal generating means OS through the delay circuit DY1 having a delay amount of 90° is set. When the change-over switch 11B is set to a change-over position 3, a mode to provide a synchronizing signal sent from the other unit to its own drive signal generating means OS through the delay circuit DY2 having a delay amount of 120° is set. Further, when the change-over switch 11B is set to a change-over position 4, a mode to provide a synchronizing signal sent from the other unit to its own drive signal generating means OS through the delay circuit DY3 having a delay amount of 240° is set. Note that BF shown in FIG. 10 represents a buffer amplifier being provided in order to send out a synchronizing signal from the synchronizing signal generator PG to the other unit.

[0044]

Likely to the example shown in this figure, when it is configured such that one inverter power source unit 10 is set in the reference phase and the other inverter power source unit 10 is set so as to operated as a unit to operate in the phase being delayed by 90° , a pulsating current I_{DC1} shown in FIG. 11A flows in the input side of one of the units, a pulsating current I_{DC2} shown in FIG. 11B flows in the input side of the other unit,

and the summed current thereof is flows into a DC power source E. Accordingly, the summed current comes to have such a wave form that the respective instant current values are averaged, that is, becomes a current wave form of containing less higher harmonics.

[0045]

With the inverter power source units of the DC reception type shown in FIG. 10, since the synchronizing signal source PG, and further the delay circuit DY1 of 90° , the delay circuit DY2 of 120° and the delay circuit DY3 of 240° are respectively provided to the respective units, they may be applied to both of the parallel operations with the inverter power source units in total of an even number and with the inverter power source units in total of an odd number. Hence, an advantage of providing the inverter power source units with a wide application range may be attained. Note that, in this example as well, it is also possible to configure the inverter power source unit such that it is provided with the delay circuits having diverse delay times, such as 360° /3 and 180° /3 when being M=3, 360° /4 and 180° /4 when being M=4, 360° /5 and 180° /5 when being M=5, 360° /6 and 180° /6 when being M=6, and so on, corresponding to the number of the inverter power source units to be used for a parallel operation.

[0046]

FIG. 12 shows an example for the inverter power source units proposed in claim 6 of this patent application, wherein M is fixed to 2. The inverter power source unit 10 of the DC reception type proposed in claim 6 is configured such that it has a DC power reception terminal T_{INDC}, installed with two

inverters INV since M is fixed to 2, and the two inverters are operated with holding a phase difference of 90° from each other.

[0047]

That is, in the same housing, a synchronizing signal having the reference phase is provided from the synchronizing signal source PG to the drive signal generating means OS that provides a drive signal to one of the two inverters INV and a synchronizing signal is provided to the drive signal generating means OS for the other inverter through the delay circuit DY1 having a delay amount of 90° . Hence, with the inverter power source unit proposed in claim 6, since the two installed inverters are operated with holding a phase difference of 90° from each other by simply connecting the unit to the DC power source E, currents with less ripple portions (containing less higher harmonics) flow into the DC power source E. Therefore, no deterioration in a battery functioning as a DC power source E will occur, and an optimum parallel operation condition may be structured.

[0048]

FIG. 13 shows an example for the inverter power source unit being proposed in claim 6, wherein M is fixed to 3. The inverter power source unit shown in this example is configured such that it is installed with three inverters in a common housing since M is fixed to 3, and the respective inverters are operated with shifting their phases by 120° from one to another.

[0049]

Accordingly, for example, a synchronizing signal outputted from the synchronizing signal generator PG is directly provided to the drive signal generating means OS in the first inverter, a synchronizing signal is provided to one of the other

drive signal generating means OS through the delay circuit DY2 having a delay amount of 120° , and a synchronizing signal is provided to the rest of the other drive signal generating means OS through the delay circuit DY3 having a delay amount of 240° .

[0050]

In this example as well, the three inverters INV are operated within the same housing in the respective phases each differing by 120° from one to another. The DC current given by adding the currents flowing into the three inverters INV becomes the averaged three-phase current and is a current containing less ripple portions. As a result, flowing of higher harmonics or a signal with a high frequency into, for example, a battery as being a DC power source E may be reduced, whereby an advantage of avoiding adverseness such as deterioration of the DC power source from occurring may be attained.

[0051]

Note that, although the inverter power source unit shown in FIG. 9 and inverter power source unit of the DC reception type shown in FIG. 13 are explained by taking an examples in which three inverters INV are installed, the number of the inverters installed in a common housing is not limited to three, and it should be appreciated that the configurations in which further more inverters in number may be installed and they may be operated with shifting their phases from one to another also fall within the range of the present invention.

[0052]

FIG. 14 shows a modification example for the drive signal generating means OS and the phase fixing means 11. This example is configured such that a wave form storage region A having a

reference phase, a wave form storage region B having a delayed phase of 90° , a wave form storage region C having a delayed phase of 120° and a wave form storage region D having a delayed phase of 240° are provided in a wave form storage means WFM, and that these storage regions A to D are changed over by means of bank change-over switches SW1 to SW4 functioning as a phase fixing means 11 to fix the storage region to be read out so that the phase of a drive signal to be supplied to the inverter is fixed.

[0053]

When employing this configuration, a synchronizing signal in the same phase having been wave-form-fairred from an AC voltage wave form of an AC generator may be provided to a phase lock loops PLL comprising the respective drive signal generating means in case of the inverter of the AC reception type, while a synchronizing signal in the same phase may be provided from a common synchronizing signal generator to the phase lock loops PLL in case of the inverter of the DC reception type. Further, as the other configuration of the drive signal generating means, a configuration to use a microcomputer to generate drive signals having the respective phases may also be employed.

[0054]

Besides, in the examples described above, all of the inverter power source units for charging lamp use are respectively provided with a boost transformer T, a filter F and a start-up circuit ST, however, the inverter power source units defined in claims 3 to 6 are directed to the inverter power source units of the type that directly send an output of the inverter to the sending terminal T_{OUT}. The inverter power source unit for charging lamp use is defined in claim 7.

[0055]

[Advantageous Effect of the invention]

As explained above, according to this invention, since a current flow with a high frequency generated in the inverter to the electric power source in an electric power source unit that concurrently operates a number of inverters can be inhibited with a simple configuration, it is possible to ravel the drawback of inverter power source units with needless of increasing the cost.

[0056]

Further, when the electric power source is an SC generator, since the power-factor of currents flowing into the generator can be improved more in comparison with inverter power source units of the conventional types, it is possible to reduce the effective capacity of a generator and to drive a load by a generator with a small capacity to thereby make a generator compact in size. Accordingly, it is effective in a great extent to use the inverter power source unit of the present invention as an electric power source to be mounted on fishing smacks and the other moving structures.

[Brief Explanation of the Drawings]

[FIG. 1] A block diagram for explaining parallel operation methods of inverters proposed in claims 1 and 2 wherein the number M of the inverters used for a parallel operation is fixed to 2;

[FIG. 2] A wave form diagram for explaining an example shown in FIG. 2;

[FIG. 3] A wave form diagram similar to FIG. 2;

[FIG. 4] A block diagram for explaining parallel operation methods of inverters proposed in claims 1 and 2 wherein the number M of the inverters used for a parallel operation is fixed to 3;

[FIG. 5] A wave form diagram for explaining the parallel operation method shown in FIG. 4;

[FIG. 6] A wave form diagram similar to FIG. 5;

[FIG. 7] A block diagram for explaining an example for an inverter power source unit proposed in claim 3 of this patent application;

[FIG. 8] A block diagram for explaining an example for an inverter power source unit proposed in claim 4 of this patent application, wherein the number M of the inverters used for a parallel operation is fixed to 2;

[FIG. 9] A block diagram for explaining an example for an inverter power source unit proposed in claim 4 of this patent application, wherein the number M of the inverters used for a parallel operation is fixed to 3;

[FIG. 10] A block diagram for explaining an example for an inverter power source unit proposed in claim 5 of this patent application;

[FIG. 11] A wave form diagram for explaining an operation of the example shown in FIG. 10;

[FIG. 12] A block diagram for explaining an example for an inverter power source unit proposed in claim 4 of this patent application, wherein the number M of the inverters used for a parallel operation is fixed to 2;

[FIG. 13] A block diagram for explaining an example for an inverter power source unit proposed in claim 4 of this patent application, wherein the number M of the inverters used for a

parallel operation is fixed to 3;

[FIG. 14] A connection diagram for explaining a prior art;

[FIG. 15] A block diagram for explaining a modification example for a drive signal generating means used for the inverter power source unit according to this invention;

[FIG. 16] A block diagram for explaining a configuration of a conventional inverter power source unit;

[FIG. 17] A wave form diagram for explaining an operation of the inverter power source unit shown in FIG. 16;

[FIG. 18] A wave form diagram of respective parts for explaining an operation of the conventional inverter power source unit shown in FIG. 16;

[FIG. 19] A block diagram for explaining an example for a drive signal generating means used for the conventional inverter power source unit shown in FIG. 16; and

[FIG. 20] A block diagram for explaining a method for raveling a drawback of conventional inverter power source units.

[Explanation for Reference signs]

10: Inverter power source unit

G: AC generator

E: DC power source

TINAC: AC reception terminal

TOUT: Sending terminal

REC: Rectification circuit

W: Smoothing circuit

INV: Inverter

T: Boost transformer

F: Filter

ST: Start-up circuit

OS: Drive signal generating means

DY1: Delay circuit having a delay amount of 90°

DY2: Delay circuit having a delay amount of 120°

DY3: Delay circuit having a delay amount of 240°

11: Phase fixing means

11A, 11B: Change-over switch